REMARKS

Claims 1, 3-11 and 13-38 are pending and were rejected. Claims 39-46 are new.

In an Office Action issued on April 7, 2005, the Examiner requested supplementation of an Amendment submitted on October 13, 2004. Specifically, the Examiner requested that Applicants supplement the Amendment filed on October 13, 2004 to specifically address why claims 39-46 are allowable over the art cited by the Examiner. In a telephone conference with the Examiner on May 6, 2005, the Examiner requested that Applicants resubmit the Amendment submitted on October 13, 2004, modified to include an explanation of why the new claims are allowable over the cited references.

Deiss Is Not An Anticipating Reference

Claims 1, 5, 10, 11, 15, 20, 30-33, 37 and 38 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 5,521,979 issued to Deiss. Applicants respectfully traverse the Examiner's contention that Deiss is an anticipating reference.

Claim 1 as amended recites:

> 1. A receiver for demultiplexing a digital data stream, the digital data stream including data packets each having a packet identifier, so as to retain only those data packets required by the receiver, the receiver comprising:
>
> an input module for receiving and processing the digital data stream;
>
> a memory for storing packet identifiers corresponding to data packets required by the receiver and separate from the input module;
>
> a first control circuit for controlling the storage in the memory of the packet identifiers;
>
> a second control circuit for extracting a packet identifier from a data packet in the digital data stream; and
>
> a third control circuit for receiving the extracted packet identifier and determining whether such matches one of the packet identifiers stored in the memory, for setting a match signal to the second control circuit responsive to a match, and for outputting an address in the memory responsive to a match,

wherein the second control circuit accesses the address in the memory to retrieve control information associated with the packet identifier and controls processing of the input data packet responsive to the match signal by the input module.

Claim 10 as amended contains similar language. The amendments to claims 1 and 10 were intended to both broaden the scope of claims 1 and 10 and to clarify a distinction between the claims and Deiss. With reference to Figure 3 of Deiss, the Examiner appears to identify: (1) antenna 10 and tuner detector 11 as the claimed input module; (2) programmable SCID register 13 and memory 18 as the claimed memory; (3) microprocessor 19 as the claimed first control circuit; (4) FEC 12, signal decryptor 16, E-code decoder 30 and smart card 31 as the claimed second control circuit; and (5) comparator 15 and memory controller 17 as the claimed third control circuit.

Deiss discloses signal component identifiers (SCID) which are stored in programmable registers (13). The SCIDs of received signal packets are compared with all the SCIDs in the programmable SCID registers. Responsive to a match the corresponding packet payload is stored in the appropriate memory area or block in memory 18, which is thus part of the circuitry for receiving the digital data stream. The Examiner appears to be suggesting that the apparatus disclosed by Deiss accesses the programmable registers (13) after a match has been found, in order to retrieve associated encryption information to decrypt the scrambled packet payload. In fact, the packet decryption described by Deiss does not require any reference to the programmable registers 13. The packet header contains a CF field and a CS field. The field CF contains a flag to indicate whether the payload of the packet is scrambled, and the field CS contains a flag which indicates which of the two alternative unscrambling keys is to be utilized to unscramble scrambled packets. See column 3, lines 5 to 9. Only the signal payloads are scrambled and the packet headers are passed by the decryptor unaltered. Whether or not a packet is to be descrambled is determined by the CF flag in the packet prefix, and how it is to be descrambled is determined by the CS flag. If no SCID match is made for a respective packet, the decryptor may simply be disabled from passing any data. See column 4, lines 47 to 55. Further, the decryptor is programmed with decryption keys provided by the smart card apparatus 31. The smart card apparatus 31 is not the programmable SCID register 13 and as such, at no stage

during the decryption of the packet does the apparatus disclosed by Deiss access the programmable SCID register 13 to retrieve control information. The CF and CS fields are not part of the SCID field and are therefore not stored in the programmable SCID register 13. See column 3, lines 2 to 5.

Thus, Deiss does not disclose "outputting an address in the memory responsive to a match, wherein the second control circuit accesses the address in the memory to retrieve control information associated with the packet identifier" or "outputting, responsive to a match, an address in the memory ... accessing ... the address in memory [and] retrieving control information ... stored at such address" as recited. The smart card 30 provides its own addressing information, and thus does not access an address output by the comparator 15 or the memory controller 17 to retrieve control information. See Deiss at column 10, lines 36-40. Further, there is no suggestion in Deiss that FEC 12, decryptor 16, E-code-decoder 30 or smart card 31 control processing of a received data packet by antenna 10 and tuner detector 11. Accordingly, Applicants respectfully submit that Deiss does not anticipate claims 1, 5 (which depends from claim 1) and 10.

Claims 11 and 20 as amended recite: "storing in a memory separate from the data stream and under the control of a first control circuit, packet identifiers of data packets required by the receiver; extracting, under the control of a second control circuit, a packet identifier from a data packet in the input digital data stream; determining, under the control of a third control circuit, whether the extracted packet identifier matches one of the stored packet identifiers; setting a match signal responsive to a match determined by the third control circuit; outputting, responsive to a match and under the control of the third control circuit, an address in the memory; accessing, under the control of the second control circuit, the address in the memory; [and] retrieving control information associated with the packet identifier and stored at such address." The Examiner relies on the analysis of claim 1 to reject claims 11 and 20. As noted above, the smart card 30 provides its own addressing information, and thus does not access an address output by the comparator 15 or the memory controller 17 to retrieve control information. See Deiss at column 10, lines 36-40. Thus, Applicants respectfully submit that Deiss does not anticipate claims 11, 15 (which depends from claim 11) and 20.

Claim 30 recites "storing control information in a first data structure; storing packet identifiers and corresponding addressing information in a second data structure ... outputting addressing information from the second data structure responsive to a match [and] retrieving ... based on the outputted addressing information, control information from the first data structure." Claim 38 similarly recites "storing, in a first data structure, control information; storing, in a second data structure, packet identifiers ... and addressing information corresponding to the packet identifiers ... outputting, responsive to a match, addressing information stored in the second data structure [and] retrieving ... based on the outputted addressing information, control information from the first data structure."

The Examiner points to the memory 18 as the first data structure and the SCID registers 13 and the memory controller 17 as the claimed second data structure. There is no indication or suggestion in Deiss that addressing information is stored in the SCID registers 13 or the memory controller 17, or that any addressing information (whether stored in SCID register 13 or otherwise) is outputted and used to retrieve control information from the memory 18. The Examiner ignores the language "outputting addressing information **from the second data structure** responsive to a match [and] retrieving ... **based on the outputted addressing information**, control information from the first data structure" as recited in the claims. Claims 31-33 and 37 depend from claim 30. Accordingly, Applicants respectfully submit that claims 30-33 and 37-38 are not anticipated by Deiss.

New claim 39 recites:

A receiver for processing a packetized digital data stream, the receiver comprising:

an input module to receive and process a data packet;

a memory;

a receiver processor to control storage of desired packet identifiers and associated control information in the memory; and

a transport controller having a transport processor to extract a packet identifier from a packet in the input module and a search engine to search the memory for a match of the extracted packet identifier to a desired packet

identifier stored in the memory, wherein responsive to a match the transport processor retrieves from the memory control information associated with the desired packet identifier stored in the memory and controls processing of the received data packet by the input module based on the retrieved control information.

Similarly, new claim 45 recites:

means for receiving a data packet in the digital data stream;

means for retrieving control information associated with a received data packet; and

means for controlling processing of a received data packet by the means for receiving a data packet.

The Examiner identifies the SCID registers 13 and the memory 18 of Deiss as the claimed memory. Applicants respectfully submit that this is an incorrect interpretation of Deiss and an unreasonable interpretation of the claim language. As discussed above, the memory 18 of Deiss is part of the input module (or the means for receiving a data packet) and Deiss does not access the SCID registers 13 to retrieve control information. Thus, Deiss does not disclose "wherein responsive to a match the transport processor retrieves from the memory control information associated with the desired packet identifier stored in the memory and controls processing of the received data packet by the input module based on the retrieved control information" as recited. Similarly, new claim 45 (the claimed means of which are limited to embodiments disclosed in the specification and their equivalents) separately recites the "means for receiving a data packet" and the "means for retrieving control information." Accordingly, Applicants respectfully submit that Deiss does not anticipate or render obvious claims 39 and 45, as well as new claims 40-44 (which depend from claim 39) and new claim 46 (which depends from claim 45).

Deiss Is Not An Appropriate Primary Reference

The Examiner rejected claims 6, 16-17 and 34-35 under 35 U.S.C. § 103(a) as rendered obvious by Deiss in view of admitted prior art. Applicants respectfully traverse the Examiner's contention that Deiss renders any of the claims obvious. Claims 6 depends from

claim 1, claims 16-17 depend from claim 11 and claims 34-35 depend from claim 30. The discussion of the MPEG-2 standard in the background section of the application does not teach or suggest the features of claims 1, 11 and 30 (and new claims 39 and 45) that are missing from Deiss. Accordingly, Applicants submit that claims 6, 16-17 and 34-35 are not rendered obvious by Deiss for the same reasons that claims 1, 11 and 30 are not anticipated by Deiss.

Dokic In View of the Manual Does Not Render the Claims Obvious

The Examiner rejected claims 1, 3-11 and 13-20 and 37 under 35 U.S.C. § 103(a) as obvious over U.S. Patent No. 5,959,659 issued to Dokic et al in view of ADSP-2100 Family User's Manual – Chapter 4: Data Transfer (the "Manual"). Applicants respectfully traverse the Examiner's contention that Claims 1, 3-11 and 13-20 are obvious over Dokic in view of the Manual. Applicants note that the Examiner did not cite the combination of Dokic and the Manual against claim 30, from which claim 37 depends.

The Examiner appears to contend that network interface 112 is the claimed input module, memory 205 and packet buffers 200 and 202 of the demultiplexer section 104 are the claimed memory, host processor 106 is the claimed first control circuit, and the controller 204 of the demultiplexer section 104 is the claimed second and third control circuits. The Examiner admits Dokic does not disclose "outputting an address in the memory responsive to a match," but contends this is disclosed by the Manual.

Dokic is not an appropriate primary reference for several reasons. First, the Examiner is using an unreasonable interpretation of the claimed memory to include the memory 205 **and** data buffers 200 and 202. Buffers 200 and 202 do not store "packet identifiers corresponding to data packets required by the receiver" and the host processor 106 does not control "storage" in the data buffers 200 and 202 of "packet identifiers", or, for that matter, of anything else (see claims 1 and 3-10). Buffers 200 and 202 are circular buffers controlled by framing logic to load **all** data packets in the transport stream, whether the packets are required or not. See Column 7, line 66 to Column 8, line 19. Thus, buffers 200 and 202 are not separate from the data stream (see claims 11 and 13-20), the input module to receive and process a data packet (see claim 39), or the means for receiving a data packet (see claim 45). Further,

demultiplexer section 102 does not control processing by the network interface 112 (claims 1 and 3-10). Thus, Dokic is not an appropriate primary reference for claims 1, 3-11, 13-20, 37 and 39-46.

As noted above, the Examiner admits that Dokic does not disclose or suggest "outputting an address", but claims this is suggested by the Manual, which describes the operation of a circular buffer. The problem with this argument is that the circular buffer of Dokic that the Examiner suggests combining with the Manual is the circular buffer 200/202, which the Examiner admits stores the "entire packet" and which as discussed above cannot be the claimed memory as recited. Accordingly, Applicants respectfully submit claims 1, 3-11, 13-20 and 39-46 are not rendered obvious by Dokic taken in combination with the Manual. Furthermore, if Dokic were modified such that the circular buffers stored either packet identifiers required by the receiver or addressing information, Dokic would not function as intended, as the stored information would be replaced (and thus lost) if the buffers were operated in a circular fashion and there would be no place to store the digital data stream as it was received if the buffers were not operated in a circular fashion or were used to store other information. Further, to the extent the address is an address of one of the buffers, it is still an address of a buffer in the data stream, and thus would not be an address in a memory separate from the data stream (claims 11 and 13-20).

Accordingly, Applicants respectfully submit that claims 1, 3-11, 13-20, 37 and 39-46 are not rendered obvious by the combination of Dokic and the Manual.

Dokic In View of Blatter Does Not Render the Claims Obvious

The Examiner also rejected claims 21-38 under 35 U.S.C. § 103(a) as obvious over Dokic in view of U.S. Patent No. 5,844,595 issued to Blatter, et al. Applicants respectfully traverse the Examiner's contention that claims 21-38 are obvious over Dokic in view of Blatter.

Claims 21 and 29 recite "a first data structure for storing addressing information that is accessed based on packet identifiers ... a second data structure for storing control information that is accessed based on addressing information extracted from the first data structure ... outputting addressing information responsive to a match ... wherein the first control circuit accesses the second data structure to retrieve control information associated with the

addressing information." Similarly, claim 30 recites ""storing control information in a first data structure; storing packet identifiers and corresponding addressing information in a second data structure ... outputting addressing information from the second data structure responsive to a match [and] retrieving ... based on the outputted addressing information, control information from the first data structure" and claim 38 similarly recites "storing, in a first data structure, control information; storing, in a second data structure, packet identifiers ... and addressing information corresponding to the packet identifiers ... outputting, responsive to a match, addressing information stored in the second data structure [and] retrieving ... based on the outputted addressing information, control information from the first data structure."

As an initial matter, the Examiner does not contend that Dokic or Blatter disclose or suggest "outputting" addressing information "responsive to a match" as claimed, and appears to expressly admit this is not disclosed or suggested by Dokic. For this reason alone, as previously pointed out by the Applicants, claims 21-38 are not rendered obvious by the combination of Dokic and Blatter. The Examiner does not address this argument in the Office Action or in the "reinterpretation" of Dokic and Blatter.

Further, the Examiner admits that Dokic does not disclose or suggest the claimed first and second data structures. The Examiner contends memory 205 of Dokic is a first data structure, without explaining how or whether it satisfies the claim limitations. The Examiner points to unit 45 of Blatter as both the first data structure and the second data structure. The Examiner does not identify how to combine unit 45 with Dokic so as to achieve the claimed invention. Further, one of skill in the art would not be motivated to combine Dokic with Blatter. Dokic is directed to "a decoder having a decoupled hardware architecture for demultiplexing and decoding a digital data stream." Dokic, Column 1, lines 6-9. Dokic specifically decouples demultiplexing from decoding the digital data stream and expressly limits the "interpretation capabilities" of the digital signal processor 102 in order to speed up the demultiplexing so data can promptly be displayed. Dokic, Column 4, lines 48-60. Modifying the digital signal processor 102 of Dokic to contain two data structures with the second data structure containing control information to be retrieved and either employed by the digital signal processor to interpret the data stream or provided to an external circuit by the digital signal processor would

defeat the purpose of limiting the capabilities of the digital signal processor in order to speed up the demultiplexing. Claims 22-28 depend from claim 21 and claims 31-37 depend from claim 30. Accordingly, Applicants submit that claims 21-38 are not rendered obvious by Dokic in view of Blatter.

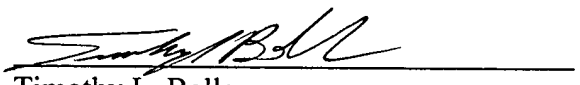
With regard to new independent claim 39, as discussed above Dokic is not an appropriate primary reference because the Examiner is using an unreasonable interpretation of the claimed memory to include the memory 205 **and** data buffers 200 and 202. The Examiner does not contend the claimed memory is taught by Blatter. Similarly, new independent claim 45 separately recites the means for receiving and the means for retrieving. In addition, as noted above, one would not be motivated to combine Dokic and Blatter because the purpose of Dokic would be defeated if the digital signal processor 102 of Dokic were modified as suggested by the Examiner.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



Timothy L. Boller
Registration No. 47,435

TLB:rg

Enclosure:
Postcard

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

858063.435/589318v1